step 88, the receiver 106 recovers an estimate RT' of the master clock signal RT from the network link clock signal RN and the received phase signal.

2. Please amend lines 16-22 at page 2 with the following amended paragraph:

Timing recovery is therefore required at the receiver side. In timing recovery, a receiver synchronizes a local clock with a master clock present at the transmitter via phase information contained directly or indirectly in the transmitted data stream. The data modulation and demodulation process that carries the data information over the link 24 may also necessitate the two sides to use a common network link clock if the link 24 is a synchronous communication link. ~~Receicer~~ Receiver synchronization to the network link clock is well understood to the skilled in the art and is not going to be described here.

3. Please amend lines 7-10 at page 7 with the following amended paragraph:

FIG. 5 illustrates a block diagram of one suitable circuit for implementing a timing generation circuit 140 suitable within the ~~transceiver~~ transmitter104 described above with reference to FIGS. 3 – 4. As will be appreciated, the timing generation circuit 140 can be useful in a variety of applications.

4. Please amend lines 6-11 at page 11 with the following amended paragraph:

The block diagram of FIG. 8 explains the required operations on the transmitter side in this enhanced embodiment of the invention. The operations on the receiver side are similar to the ones explained before based on the block diagram of FIG. 7. The difference in this embodiment is that the RN divider ~~260~~ 250 is fixed to its nominal value 184, while only the divider 260 is allowed to vary around its nominal value of 233 by +/-1.